**Remarks/Arguments**

The Examiner is thanked for the thorough examination and search of the subject.

Claims 43-74, 83, 84 and 89-102 are pending; Claims 43, 59, 64 and 89 have been currently amended; Claims 1-42, 75-82 and 85-88 have been canceled. No new matter is believed to have been added.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicant respectfully traverses the rejections for at least the reasons set forth below.

**Response to Claims 43-63**

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As currently amended, independent Claim 43 is recited below:

43. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a first dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said first dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure, and said first contact point is at a

bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said metallization structure, and said second contact point is at a bottom of said second opening, wherein said first and second contact points are separated from each other by an insulating material, wherein said passivation layer comprises an insulating nitride layer; and

a circuit trace over said passivation layer and on said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, and wherein said circuit trace is connected to said resistor through said first opening.

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*Reconsiderations of Claims 43 and 48-53 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380), of Claims 54-59 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Erdejac et al. (U.S. Pat. No. 6,235,101), of Claims 60-63 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Sasagawa et al. (U.S. Pat. No. 6,486,530) or over Lin et al. in view of Woolery et al., Erdejac et al. and Sasagawa et al., of Claims 44-46 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Leidy (U.S. Pub. No. 2003/0155570), and of Claims 45 and 47 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Simila (U.S. Pub. No. 2003/0183332) are requested in accordance with the following remarks.*

Applicant respectfully asserts that the chip structure currently claimed in Claim 43 patentably distinguishes over the citations by Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380).

The Examiner considers that "Lin discloses a chip structure

comprising: ..... a resistor in said silicon substrate" and that "One of ordinary skill in the art at the time the invention was made would interpret "transistors and other devices" to include resistors, as is supported by many references, including the secondary reference Woolery which discloses a silicon substrate with resistors (440) and resistors (420) see Fig. 4E. Further, other references disclosing metallization also disclose transistors and resistors within a substrate, for example U.S. Pat. No. 6,261,944 to Mehta et al. (col. 3, lines 45-57) and U.S. Pat. No. 5,328,553 to Poon (col. 5, lines 33-38)" *~ See lines 20-23 on page 2 and lines 9-15 on page 12, in the last Office Action mailed Dec. 23, 2008 ~*

Applicant respectfully traverses the Examiner's opinion because it is believed that Lin et al. fail to disclose that a chip structure comprises a resistor in a silicon substrate. Even though Woolery et al. disclose that a device comprises a resistor 420, Mehta et al. disclose that a device layer 12 comprises a resistor, and Poon discloses that a device comprises a resistor, Woolery et al. disclosure, Mehta et al.'s disclosure and Poon's disclosure are not Lin et al.'s disclosure. *~ See Fig. 4E in U.S. Pat. No. 6,528,380 , Fig. 1 and col. 3, lines 38-57 in 6,261,944 and col. 5, lines 33-38 in U.S. Pat. No. 5,328,553 ~* Lin et al. fail to teach what kind of other devices could be, and thus the wording of "transistors and other devices" can not be deemed as the disclosure including a resistor.

The Examiner considers that Lin et al.'s circuit trace (26/22/36/28/38) is connected to a resistor through Lin et al.'s first opening 16. *~ See line 17 of page 3 through line 3 of page 4, in the last Office Action mailed Dec. 23, 2008 ~*

Applicant respectfully traverses the Examiner's opinion because Applicant can not find that Lin et al.'s circuit trace (26/22/36/28/38) is connected to a resistor through Lin et al.'s first opening 16. If the Examiner does consider that Lin et al.'s circuit trace (26/22/36/28/38) is connected to a resistor through Lin et al.'s first opening 16, showing the path between Lin et al.'s circuit trace (26/22/36/28/38) and a

resistor is respectfully requested.

Withdrawal of rejection under 35 U.S.C.103(a) to Claim 43 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 43 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 44-63 patently define over the prior art as well.

**Response to Claims 64-74, 83 and 84**

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As currently amended, independent Claim 64 is recited below:

64. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said metallization structure, and said second contact point is at a bottom of said second opening, wherein said first and second contact points are separated from each other by an insulating

material, wherein said passivation layer comprises an insulating nitride layer; and

a circuit trace over said passivation layer and on said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor through said first opening, and wherein said circuit trace comprises a titanium-containing layer and a gold layer over said titanium-containing layer.

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*Reconsiderations of Claims 64, 69-74, 83 and 84 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380) and Sasagawa et al. (U.S. Pat. No. 6,486,530) or over Lin et al. in view of Woolery et al., Erdejac et al. (U.S. Pat. No. 6,235,101) and Sasagawa et al., of Claims 65-67 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Sasagawa et al., further in view of Leidy (U.S. Pub. No. 2003/0155570), and of Claims 66 and 68 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Sasagawa et al., further in view of Simila (U.S. Pub. No. 2003/0183332) are requested in accordance with the following remarks.*

Applicant respectfully asserts that the chip structure currently claimed in Claim 64 patentably distinguishes over the citations by Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380) and Sasagawa et al. (U.S. Pat. No. 6,486,530).

The Examiner considers that "Lin discloses a chip structure comprising: ..... a resistor in said silicon substrate" and that "One of ordinary skill in the art at the time the invention was made would interpret "transistors and other devices" to include resistors, as is supported by many references, including the secondary reference Woolery which discloses a silicon substrate with resistors (440)

and resistors (420) see Fig. 4E. Further, other references disclosing metallization also disclose transistors and resistors within a substrate, for example U.S. Pat. No. 6,261,944 to Mehta et al. (col. 3, lines 45-57) and U.S. Pat. No. 5,328,553 to Poon (col. 5, lines 33-38)" *~ See lines 17-20 on page 7 and lines 9-15 on page 12, in the last Office Action mailed Dec. 23, 2008 ~*

Applicant respectfully traverses the Examiner's opinion because it is believed that Lin et al. fail to disclose that a chip structure comprises a resistor in a silicon substrate. Even though Woolery et al. disclose that a device comprises a resistor 420, Mehta et al. disclose that a device layer 12 comprises a resistor, and Poon discloses that a device comprises a resistor, Woolery et al. disclosure, Mehta et al.'s disclosure and Poon's disclosure are not Lin et al.'s disclosure. *~ See Fig. 4E in U.S. Pat. No. 6,528,380 , Fig. 1 and col. 3, lines 38-57 in 6,261,944 and col. 5, lines 33-38 in U.S. Pat. No. 5,328,553 ~* Lin et al. fail to teach what kind of other devices could be, and thus the wording of "transistors and other devices" can not be deemed as the disclosure including a resistor.

The Examiner considers that Lin et al.'s circuit trace (26/22/36/28/38) is connected to a resistor through Lin et al.'s first opening 16. *~ See line 17 of page 8 through line 3 of page 9, in the last Office Action mailed Dec. 23, 2008 ~*

Applicant respectfully traverses the Examiner's opinion because Applicant can not find that Lin et al.'s circuit trace (26/22/36/28/38) is connected to a resistor through Lin et al.'s first opening 16. If the Examiner does consider that Lin et al.'s circuit trace (26/22/36/28/38) is connected to a resistor through Lin et al.'s first opening 16, showing the path between Lin et al.'s circuit trace (26/22/36/28/38) and a resistor is respectfully requested.

The Examiner considers that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to include the

different circuit trace and metallization layers of Sasagawa in order to optimize the device performance under thermal stress". ~ *See lines 14-17 on page 9, in the last Office Action mailed Dec. 23, 2008* ~

Applicant respectfully traverse the Examiner's opinion because it would not have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin et al.'s circuit trace (26/22/36/28/38) with Sasagawa et al.'s metallization structure (109/110/111A/111B/111C). Lin et al.'s circuit trace is composed of plugs 36 and 38 and an upper metal layer 28 not integrated with the plugs 36 and 38. Sasagawa et al.'s metallization structure (109/110/111A/111B/111C) is composed of plugs in Sasagawa et al.'s dielectric film layer 108 and an upper metal layer, integrated with the plugs, on Sasagawa et al.'s dielectric film layer 108, which is significantly different from Lin et al.'s circuit trace (36/28/38). The metallization of Lin et al.'s circuit trace (36/28/38) with the upper metal layer 28 not integrated with the plugs 36 and 38 is believed not to be attained using the process for forming Sasagawa et al.'s metallization structure (109/110/111A/111B/111C) due to Sasagawa et al.'s metallization structure (109/110/111A/111B/111C) with the upper metal layer integrated with the plugs. Therefore, Sasagawa et al.'s metallization structure (109/110/111A/111B/111C) is believed not to be applied to Lin et al.'s circuit trace (36/28/38).

Withdrawal of rejection under 35 U.S.C.103(a) to Claim 64 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 64 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 65-74, 83 and 84 patently define over the prior art as well.

**Response to Claims 89-102**

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As currently amended, independent Claim 89 is recited below:

89. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said metallization structure, and said second contact point is at a bottom of said second opening, wherein said first and second contact points are separated from each other by an insulating material, wherein said passivation layer comprises an insulating nitride layer; and

a circuit trace over said passivation layer and on said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor through said first opening, and wherein said circuit trace comprises a copper layer.

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*Reconsiderations of Claims 89 and 94-99 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al.*

*(U.S. Pat. No. 6,528,380), of Claims 100-102 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Sasagawa et al. (U.S. Pat. No. 6,486,530) or over Lin et al. in view of Woolery et al., Erdejac et al. (U.S. Pat. No. 6,235,101) and Sasagawa et al., of Claims 90-92 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Leidy (U.S. Pub. No. 2003/0155570), and of Claims 91 and 93 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Simila (U.S. Pub. No. 2003/0183332) are requested in accordance with the following remarks.*

Applicant respectfully asserts that the chip structure currently claimed in Claim 89 patentably distinguishes over the citations by Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380).

The Examiner considers that "Lin discloses a chip structure comprising: ..... a resistor in said silicon substrate" and that "One of ordinary skill in the art at the time the invention was made would interpret "transistors and other devices" to include resistors, as is supported by many references, including the secondary reference Woolery which discloses a silicon substrate with resistors (440) and resistors (420) see Fig. 4E. Further, other references disclosing metallization also disclose transistors and resistors within a substrate, for example U.S. Pat. No. 6,261,944 to Mehta et al. (col. 3, lines 45-57) and U.S. Pat. No. 5,328,553 to Poon (col. 5, lines 33-38)" *~ See lines 11-14 on page 4 and lines 9-15 on page 12, in the last Office Action mailed Dec. 23, 2008 ~*

Applicant respectfully traverses the Examiner's opinion because it is believed that Lin et al. fail to disclose that a chip structure comprises a resistor in a silicon substrate. Even though Woolery et al. disclose that a device comprises a resistor 420, Mehta et al. disclose that a device layer 12 comprises a resistor, and Poon discloses that a device comprises a resistor, Woolery et al. disclosure, Mehta et al.'s disclosure

and Poon's disclosure are not Lin et al.'s disclosure. ~ *See Fig. 4E in U.S. Pat. No. 6,528,380 , Fig. 1 and col. 3, lines 38-57 in 6,261,944 and col. 5, lines 33-38 in U.S. Pat. No. 5,328,553* ~ Lin et al. fail to teach what kind of other devices could be, and thus the wording of "transistors and other devices" can not be deemed as the disclosure including a resistor.

The Examiner considers that Lin et al.'s circuit trace (26/22/36/28/38) is connected to a resistor through Lin et al.'s first opening 16. ~ *See lines 10-20 on page 5, in the last Office Action mailed Dec. 23, 2008* ~

Applicant respectfully traverses the Examiner's opinion because Applicant can not find that Lin et al.'s circuit trace (26/22/36/28/38) is connected to a resistor through Lin et al.'s first opening 16. If the Examiner does consider that Lin et al.'s circuit trace (26/22/36/28/38) is connected to a resistor through Lin et al.'s first opening 16, showing the path between Lin et al.'s circuit trace (26/22/36/28/38) and a resistor is respectfully requested.

Withdrawal of rejection under 35 U.S.C.103(a) to Claim 89 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 89 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 90-102 patently define over the prior art as well.

Conclusion

Some or all Claims are believed to be in condition for Allowance, and that is so requested.

Sincerely yours,

/Winston Hsu/ Date: 03/17/2009

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